REMARKS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-20 are presently active in this case. The present Amendment amends Claims 1-12 and adds new Claims 13-20.

In the outstanding Office Action, Claims 1, 4, 5 and 8 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kawai et al. (U.S. Patent No. 5,715,436, herein referred as "Kawai"). Claims 2, 3, 6, 7, 9 and 10 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kawai in view of Harney (U.S. Patent No. 5,522,080). Claims 11 and 12 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kawai in view of Harney as applied to claim 2 above, and further in view of Gove et al. (U.S. Patent No. 6,070,003, herein referred as "Gove").

First, Applicants wish to thank Examiner Burleson and Supervisor Williams for the courtesy of an interview granted to Applicants' representative on November 10, 2004, at which time the outstanding issues in this case were discussed. Amendments and arguments similar to the ones developed in the present amendment were discussed. The Examiner indicated that he would reconsider the outstanding grounds for rejection upon formal submission of a response.

Applicants have noticed that the Information Disclosure Statement filed on December 14, 2000 has not been acknowledged as having been considered by the Examiner. Applicants respectfully request the Examiner to acknowledge the IDS in the next Office Action.

In order to clarify Applicants' invention, Claims 1-12 are amended to better comply with U.S. claim drafting practice and to correct minor informalities. As discussed during the interview, Claims 1, 5, 10 and 12 are amended to specify that a memory switch is configured to selectively connect the plurality of memories with the data operation unit. Claims 9 and 11

are amended to specify that the memories are local memories used for an image processing conducted by the SIMD type data operation unit. Further, Claims 1-3, 5-7 and 9-12 are amended to recite "a plurality of memory controllers."

New Claims 13-16 are added to vary the scope of protection. New Claims 13 and 14 depend upon Claims 9 and 11 respectively and recite that "said SIMD type data operation unit does not access an external memory outside of the programmable image processing unit." This feature finds non-limiting support in Applicants' disclosure, for example at page 30, lines 3-15 with corresponding Fig. 3. New Claims 15 and 16 depend upon Claims 1 and 5 respectively and recite that "said least one auxiliary operation means performs an IIR (Infinite Impulse Response) type filter image processing." These features find non-limiting support in Applicants' disclosure, for example at page 24, lines 12-25. New Claims 17 and 18 depend upon Claim 1 and 5 respectively and recite that "said bus switch is configured to change a bus width of said plurality of data buses allotted to said image formation operation executed in said data operation unit." These features find non-limiting support in Applicants' disclosure, for example at page 28, lines 10-20. New Claims 19 and 20 depend upon Claim 1 and 5 respectively and recite that "said memory switch adapts a data format for said image data processed by said data operation unit." These features find non-limiting support in Applicants' disclosure, for example at page 27, line 22 to page 28, line 3. Therefore, new Claims 13-20 are not believed to raise a question of new matter.[1]

In response to the rejection of Claims 1, 4, 5 and 8 under 35 U.S.C. § 102(b), Applicants respectfully request reconsideration of this rejection and traverse the rejection as discussed next.

Briefly recapitulating, Applicants' invention, as recited in Claims 1 and 5, relates to an image processing apparatus, including a programmable image processing unit, wherein the

[1] See MPEP 2163.06 stating that "information contained in any one of the specification, claims or drawings of the application as filed may be added to any other part of the application without introducing new matter."

programmable image processing unit includes a SIMD type data operation unit, a plurality of memories and a memory switch configured to selectively connect the plurality of memories with the data operation unit. The programmable image processing unit further includes a plurality of data buses, and a bus switch configured to control a connection between the plurality of data buses and the SIMD type data operation unit. As explained in Applicants' specification at page 2, line 22 to page 3, line 6 with corresponding Fig. 3, Applicants' invention improves upon conventional image processing apparatuses because it is capable of controlling an overall system by flexibly corresponding to a data format in each operation mode among a plurality of operation modes.

Turning now to the applied prior art, Kawai discloses a high speed programmable image processing circuit, including SIMD type processing units arranged in parallel and connected to output lines of data memories.[2] As discussed during the interview, however, Kawai fails to teach a memory switch configured to selectively connect the plurality of memories with a data operation unit, as recited in amended Claims 1 and 5.

Furthermore, Kawai fails to teach a bus switch configured to control a connection between the plurality of data buses and the data operation unit. On Fig. 5, Fig. 19, Fig. 20 and Fig. 21 of Kawai it can be seen that the data memories 2-1 to 2-n are directly connected with data buses 25-1 to 25-n to the corresponding processing units 1-1 to 1-n. Additionally, Kawai explicitly teaches that SIMD type processing units are provided in corresponding relation to outputs of the plurality of data memories[3] and that the first to third data memories are associated respectively with the SIMD type first to third processing units.[4]

Applicants respectfully traverse the position that the Kawai's s*elector circuits* (40-1 and 40-2) read on a bus switch configured to control connection between the plurality of data

[2] See Kawai in the Abstract.
[3] See Kawai at column 3, lines 2-5.
[4] See Kawai at column 9, lines 52-56.

buses and the data operation unit.[5] The Kawai reference expressively states that the control means and the selector means control the input data signal written to and read from the data memories. Furthermore, Kawai teaches that if the selector means connects the input of the data memory to the output of the DMA transfer control means, then the input data signal is transferred from the output of the DMA transfer control means directly to the data memory.[6] In other words, Kawai's selector circuits allow data to be transferred via DMA from the external memory to the local data memories associated with the SIMD type processor units. In Kawai, the connection between the local data memories and the SIMD type processor units is a direct connection and no bus switches are disclosed. The selector circuit as taught by Kawai ***is not*** a bus switch configured to control a connection between the plurality of data buses and the data operation unit, as recited in Applicants' claims. Furthermore Kawai's selector circuits do not change a bus width of the plurality of data buses allotted to the image formation operation executed in the data operation unit, as recited in new dependent Claims 17 and 18.

Therefore, the prior art fails to teach or suggest every feature recited in Applicants' claims, so that Claims 1, 4, 5, 8, 17 and 18 are patentably distinct over the prior art. Accordingly, Applicants respectfully traverse, and request reconsideration of, the rejections based on the Kawai patent.[7]

Furthermore, the image processing apparatus, as recited in Applicants' Claim 1, includes plurality of memories (for example RAMs 307) used for image processing, a plurality of memory controllers (for example 305a) that control each of the plurality of memories, and the memory switches (for example switches 301a, 301b, 301c and 301d)

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[5] See in outstanding Office Action, on page 6, lines 1-4.
[6] See Kawai at column 5, lines 52-63.
[7] See MPEP 2131: "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," (Citations omitted) (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

configured to selectively select the memories.[8] Therefore, with the present invention it is possible to adapt the size and the use of the plurality of memories, and a flexible use of the plurality of memories can be obtained.

The Kawai system describes a plurality of data memories.[9] However, Kawai fails to teach or suggest the controlling of a plurality of memories by *a plurality of memory controllers*. Therefore, the present invention recites features that are not disclosed nor taught by the cited prior art references.

In response to the rejection of Claim 10 under 35 U.S.C. § 103(a) and Claim 12 under 35 U.S.C. § 103(a), Applicants respectfully request reconsideration of these rejections and traverse the rejections as discussed next.

As discussed above, the Kawai patent does not disclose the claimed memory switch configured to selectively connect the plurality of memories with the data operation unit. Further, Kawai fails to disclose the claimed bus switch configured to control a connection between the plurality of data buses and the SIMD type data operation unit. Harney also fails to disclose the above features, as next discussed.

The Harney patent recites that local memory ports 361a-n and global memory ports 363a-n, together, provide each execution data path 358a-n with a ***dual port architecture*** to permit each execution unit 360a-n to access its respective local memory 362a-n simultaneously with data transfer between local memories 362a-n and memories 364, 366. Additionally, Harney explains that no execution unit 360a-n may directly access any local memory 262a-n except its own.[10] Reading Harney, a person of ordinary skill in the art would understand that ***a dual port architecture*** **of** the image processor is not a ***bus switch*** controlling a connection between the plurality of data buses and the data operation unit,[11] as

[8] See Applicants' specification at page 23, line 7 and in Fig. 3.
[9] See Kawai from column 9, line 32 to column 10, line 8.
[10] See Harney, for example, at column 5, lines 25-27.
[11] See Harney, for example, at column 13, lines 5-7.

recited in Applicants' claims. Therefore, even if the combination of the Kawai and Harney is assumed to be proper, the combination fails to teach every element of the claimed invention. Accordingly, Applicants respectfully traverse, and request reconsideration of, this rejection based on these patents.[12]

In response to the rejection of Claims 2, 3, 6 and 7 under 35 U.S.C. § 103(a), the Claims 2 and 3 depend upon independent Claim 1 and Claims 6 and 7 depend upon independent Claim 5, so that the rejection is traversed for the same reasons set forth above regarding Claims 1 and 5. Applicants therefore request reconsideration of this rejection.

In response to the rejections of Claim 9 under 35 U.S.C. § 103(a) and Claim 11 under 35 U.S.C. § 103(a), Applicants respectfully request reconsideration of these rejections and traverse the rejections as discussed next.

Kawai discloses a high speed programmable image processing circuit, including SIMD type processing units arranged in parallel and connected to output lines of data memories. The Kawai patent, however, fails to teach or suggest Applicants' claimed image processing method comprising the step of selectively connecting the local memories to the data operation unit by using the plurality of memory controllers and the memory switch and thereby changing a memory capacity allotted to each image formation operation. In particular, and as acknowledged by the outstanding Office Action,[13] Kawai fails to teach or suggest the claimed step of connecting the local memories to the data operation unit selectively by using the plurality of memory controllers and the memory switch.

The outstanding Office Action rejects Applicants' Claims 9 and 11 based on the proposition that Harney discloses the above feature,[14] and that it would have been obvious to

[12] See MPEP 2142 stating, as one of the three "basic criteria [that] must be met" in order to establish a *prima facie* case of obviousness, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations," (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."
[13] See in the outstanding Office Action on page 8, lines 19-20.
[14] See in the outstanding Office Action on page 8, line 20 to page 9, line 5.

modify Kawai by importing this feature from Harney to arrive at Applicants' claimed invention. Applicants respectfully submit, however, that Harney fails to disclose the above step of selectively connecting the local memories to the data operation unit by using the plurality of memory controllers and the memory switch and thereby changing a memory capacity allotted to each image formation operation, as next discussed.

The outstanding Office Action relies on the Harney's text at column 13, lines 31-47 and Fig. 3. In this passage, Harney recites that access to global memory 366 is shared by all execution data paths 358a-n within single-instruction multiple data image processor 300. Furthermore, Harney states that the data transfer by way of local memory ports 361a-n is distinguished from transfers by way of transfer ports 363a-n under the control of block transfer controller 368.[15] Reading the Harney patent, a person of ordinary skill in the art would understand that the execution units either access the local memories 362a-n directly by way of the local data buses 361a-n, or accesses the global memory 364 or 366 through the block transfer control module 368. Accessing global memory 366 by way of memory interface 370 and global port 376 under the control of block transfer controller 368,[16] as taught by Harney, is not selectively connecting the local memories to the data operation unit by using the plurality of memory controllers and the memory switch and thereby changing a memory capacity allotted to each image formation operation, as recited in Claim 11. As explained in Harney, each execution unit 360a-n of each respective execution data path 358a-n directly accesses its own local memory.[17] Accordingly, accessing global memory 366 with the block transfer controller 368 and memory interface 370 in Harney ***is not*** selectively connecting the local memories to the data operation unit by using the plurality of memory controllers and the memory switch, as recited in Applicants' claims. Therefore, even if the

[15] See Harney at column 13, lines 11-14.
[16] See Harney at column 13, lines 48.
[17] See Harney at column 13, lines 1-3.

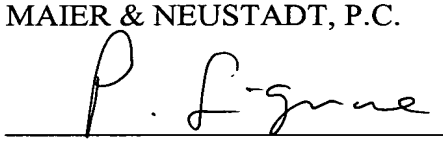
combination of the Kawai and Harney is assumed to be proper, the combination fails to teach every element of the claimed invention. Accordingly, Applicants respectfully traverse, and request reconsideration of, these rejections based on these patents.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1-20 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599

Philippe J.C. Signore
Registration No. 43,922

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)

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